[Total No. of Questions - 9] [Total No. of Printed Pages - 2]
(2125)

15258

B. Tech 7th Semester Examination

Digital System Design (OS)

EC(ID)-7005

Time : 3 Hours **Max. Marks : 100**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : Attempt five questions in all selecting one question from each of the section A, B, C & D of the question paper and all the questions from Section E. Use of Non Programmable calculators is allowed.

SECTION - A

1. Discuss various types of Data Objects, Data types, Classes and Operators used in VHDL. (20)

2. Write a programme for Full Adder in Behavioural, Data Flow and Structural Style of Modelling. (20)

SECTION - B

3. With the help of Case Statement, Write a code for 8 : 1 MUX by using 2 : 1 MUX. (20)

4. Describe the Assignment, Conditional and Sequential Statements with suitable examples. (20)

SECTION - C

5. Implement 4 - bit ring counter using VHDL Code. (20)

6. Implement the circuit for 16 : 1 Multiplexer using VHDL Code. (20)

[P.T.O.]

SECTION - D

7. (a) Differentiate between PAL and PLA with suitable examples. (10)

   (b) How Programming Logic Devices can be used in VHDL? State with some example. (10)

8. (a) What are two design entry methods for programming PLDs and FPGAs? (10)

   (b) How CPLD differs from SPLD? (10)

SECTION - E

9. Answer the following:

   (a) Differentiate between GAL & PEEL.

   (b) State various features of VHDL.

   (c) Define Entity & Architecture with citing their Syntax.

   (d) Explain the use of Generics in VHDL.

   (e) What is logic Synthesis in HDL? (5×4=20)